White LED Driver for LCD Monitors Backlighting

Check for Samples: TPS61199

FEATURES

- 8V to 30V Input Voltage
- Integrated High-Power Boost Controller
- Adaptive Boost Output for LED Voltages
- Drive up to Eight LED Strings in Parallel
- Maximum 70 mA for Each LED String
- 3% Current Matching Between Strings
- 5000:1 PWM Dimming Ratio at 200Hz
- MOSFET Over-current Protection
- Programmable LED Short Protection
- Adjustable LED Open Protection
- Thermal Shutdown Protection
- 20-pin SOP Package and TSSOP Package with PowerPAD™

APPLICATIONS

- Monitor LCD Backlight
- LCD TV Backlight
- General LED Lighting

DESCRIPTION

The TPS61199 provides highly integrated solutions for large size LCD backlighting. This device integrates a current-mode boost controller and eight current sinks for driving up to eight LED strings with multiple LEDs in series. Each string has an independent current regulator with current matching between strings reaching 3% regulation accuracy. The IC adjusts the boost controller's output voltage automatically to provide only the voltage required by the LED string with the largest forward voltage drop plus the minimum required voltage at that string's IFBx pin, thereby optimizing the driver's efficiency.

The TPS61199 provides PWM brightness dimming with an external PWM signal. The PWM signal's maximum frequency can be as high as 22kHz. Dimming ratios up to 5000:1 can be achieved with 200Hz PWM signal. The TPS61199 integrates over current protection for the switch FET, soft startup, LED short protection, LED open protection, and over temperature shutdown protection. The TPS61199 device is available in 20-pin SOP and HTSSOP package.

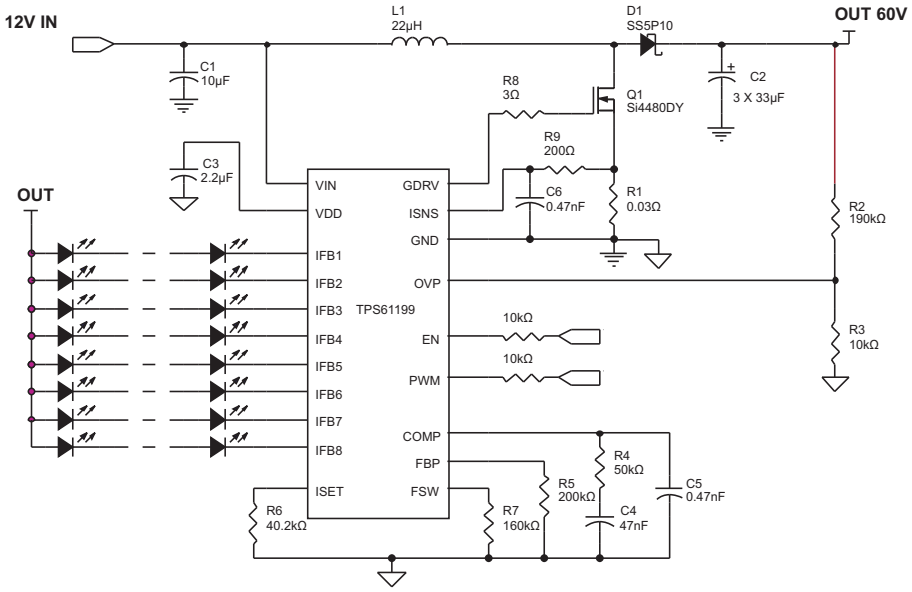


Figure 1. Typical Application of TPS61199

Table 1. PACKAGE INFORMATION(1)

PACKAGE	PART NUMBER(2)
SOP – 20	TPS61199NS
HTSSOP – 20	TPS61199PWP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document; or, see the TI Web site at www.ti.com.
(2) The SOP and HTSSOP package are available in tape and reel. Add R suffix (TPS61199PWPR / TPS61199NSR) to order quantities of 2000 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage Range	Pin VIN(2)	–0.3	33	V
	Pin IFB1 to IFB8(2)	–0.3	30	
	Pin EN and PWM(2)	–0.3	20	
	Pin ISET, ISNS and OVP(2)	–0.3	3.6	
	All other pins(2)	–0.3	7	
HBM ESD rating			2	KV
Continuous Power Dissipation		See Thermal Information Table		
Operating Junction Temperature Range		–40	+150	°C
Storage Temperature Range		–65	+150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	NOM	MAX	UNIT
L1	Inductor	10	22	47	µH
C1	Input capacitor	10			µF
C2	Output capacitor	10	33	100	µF
f_{PWM}	PWM dimming frequency	0.1		22	KHz
t_{PWM}	Rising/falling edge of PWM signal			1	µsec
f_{BOOST}	Boost regulator switching frequency	300		800	kHz
T_A	Operating ambient temperature	–40		85	°C

(1) Customers need to verify the component values in their application if the values are different from the recommended values.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61199 NS 20 PINS	TPS61199 PWP 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	69.4	46.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	36.4	48.2	
θ_{JB}	Junction-to-board thermal resistance	37.3	22.1	
ψ_{JT}	Junction-to-top characterization parameter	11.0	3.4	
ψ_{JB}	Junction-to-board characterization parameter	36.8	13.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	2.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

VIN = 12V; T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

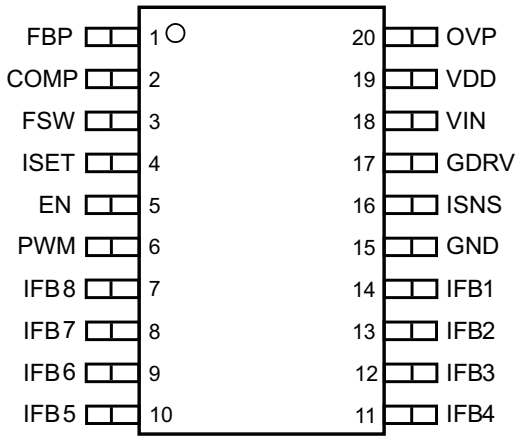
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
VIN	Input voltage range		8		30	V
V_{UVLO_VIN}	Under voltage lockout threshold	VIN falling		6.5	7	V
V_{VIN_SYS}	VIN hysteresis	VIN rising		300		mV
I_{q_VIN}	Operating quiescent current into Vin	EN=high; PWM = low; no switching, VIN=30V			1.5	mA
I_{SD}	Shutdown current				10	µA
VDD	Internal regulation voltage	Output current of VDD = 15mA	5.7	6.0	6.3	V
EN and PWM						
V_H	Logic high threshold on EN,PWM,	VIN = 8V to 30V	2.0			V
V_L	Logic Low threshold on EN,PWM,	VIN = 8V to 30V			0.8	V
R_{PD}	Pull down resistor on EN, PWM		400	800	1600	kΩ
CURRENT REGULATION						
V_{ISET}	ISET pin voltage		1.204	1.229	1.253	V
K_{ISET}	Current multiple $I_{IFB(AVG)}$/Iset	I_{ISET} = 30µA; IFB = 450mV		1990		
IFB	Current accuracy to $I_{IFB(AVG)}$	I_{ISET} = 30µA; IFB = 450mV	-2%		2%	
$IFB_{(BR)}$ (1)	Current matching	I_{ISET}= 30µA; IFB = 450mV			3%	
IFB_{leak}	IFB pin leakage current	IFB voltage = 30V; PWM = low	10	25	45	µA
I_{IFB_max}	Current sink max output current	IFB = 450mV	70			mA
OSCILLATOR						
F_{OSC}	Switching frequency	R = 100 kΩ	0.66	0.8	0.94	MHz
		R = 160 kΩ	0.44	0.5	0.56	
V_{FSW}	FSW pin reference voltage			1.229		V
$Duty_{max}$	Maximum duty cycle	FSW= 500 kHz	90%	94%		
t_{skip}	Minimum pulse width for skip cycle mode			200		ns
GATE DRIVER and OVER CURRENT LIMIT						
$R_{GDRV(SRC)}$	Gate driver impedance when sourcing	V_{GDRV} = 6V, I_{GDRV} = 20mA		2		Ω
$R_{GDRV(SNK)}$	Gate driver impedance when sinking	V_{GDRV} = 6V, I_{GDRV} = 20mA		1.5		Ω
V_{ISNS}	Switch current limit detection threshold	VIN = 8V to 30V	120	160	180	mV
PROTECTION						
V_{CLAMP}	Output overvoltage threshold at OVP pin		2.77	2.95	3.13	V
I_{FBP}	LED short across protection bias current multiple I_{FBP}/I_{ISET}	VFBP = 1V	0.23	0.25	0.27	
V_{OVP_IFB}	IFB overvoltage threshold		26.5		29.5	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C

(1) Current matching = (I_{MAX} – I_{MIN})/ I_{AVG}

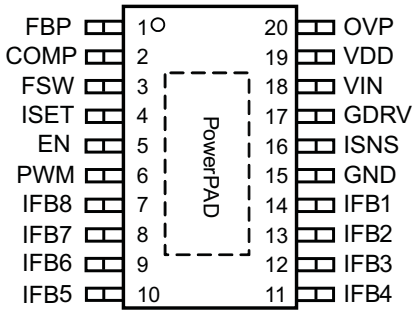
DEVICE INFORMATION

TOP VIEW

SOP - 20 (NS)



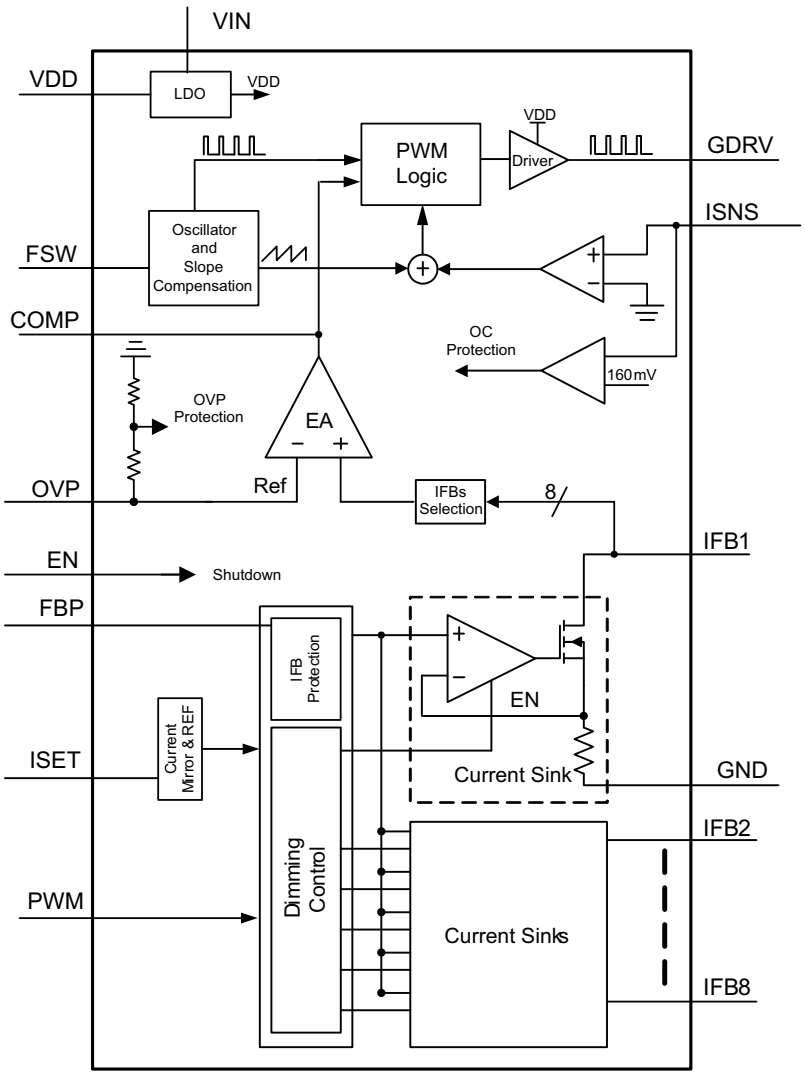
HTTSOP - 20 (PWP)



PIN ASSIGNMENTS

PIN		DESCRIPTION
NAME	NO.	
VDD	19	Internal regulator output pin. Connect a 2.2µF capacitor between this pin to GND.
EN	5	Enable/disable Pin. High = IC is enabled; low = IC is disabled.
FSW	3	Boost switching frequency selection pin. Connect a resistor to set the frequency between 300kHz to 800 kHz
PWM	6	PWM dimming signal input pin. The frequency must be in the range of 100Hz to 22 kHz
ISET	4	Full-scale LED current selection pin. Connect a resistor to program LED current for each string
IFB1 to IFB8	7, 8, 9, 10, 11 12, 13, 14	Regulated current sink input pins.
GND	15	Ground pin
COMP	2	Loop compensation pin. Connect an RC network to make loop stable. See the relevant application information section.
ISNS	16	External MOSFET current sense positive input pin.
GDRV	17	External Switch MOSFET gate driver output pin.
OVP	20	Over voltage protection pin. See the relevant application information section
FBP	1	LED short-across protection threshold program pin. See the relevant application information section
VIN	18	Supply input pin. This pin can be tied to a voltage different from the power stage input.
PowerPAD in TPS61199PWP		The PowerPAD pad must be soldered to the ground. If possible, use thermal vias to connect to top and internal ground plane layers for ideal power dissipation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Figure 1 as test circuit, and L = CDRH127/HPNP- 220M, R6 = 41kΩ, unless otherwise noted		
DESCRIPTION		**FIGURES**
Dimming efficiency	17LEDs in series; 200Hz dimming frequency;	Figure 2
Dimming efficiency	13LEDs in series; 200Hz dimming frequency;	Figure 3
Dimming linearity	17LEDs in series; VIN = 12V;	Figure 4
Dimming with short on time	17LEDs in series; VIN = 12V;	Figure 5
Current matching	17LEDs in series; VIN = 12V;	Figure 6
Dimming waveform	17LEDs in series; VIN = 12V; 200Hz with 1% duty cycle	Figure 7
Dimming waveform	17LEDs in series; VIN = 12V; 22kHz with 5% duty cycle	Figure 8
Startup waveform	17LEDs in series; VIN = 12V; 200Hz with 50% duty cycle	Figure 9
Shutdown waveform	17LEDs in series; VIN = 12V; 200Hz with 50% duty cycle	Figure 10

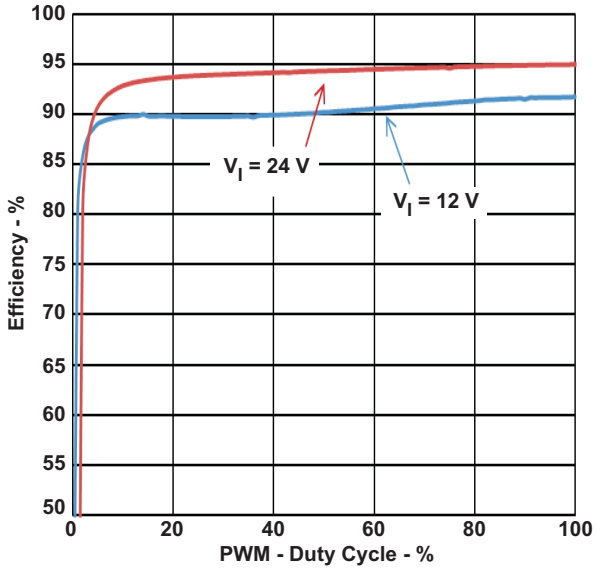


Figure 2. Dimming Efficiency

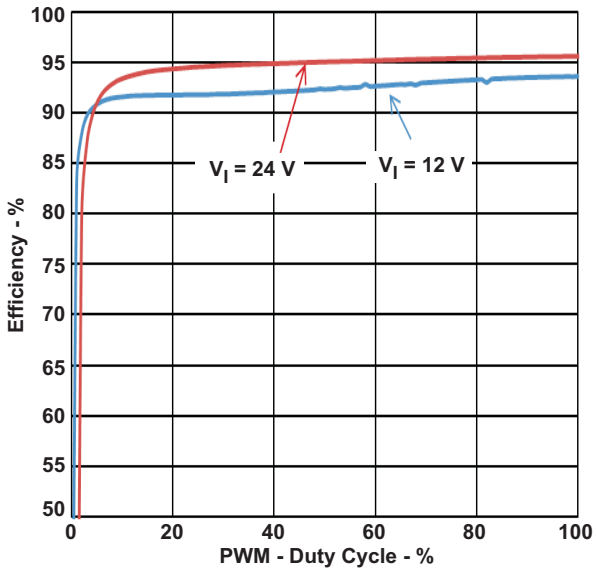


Figure 3. Dimming Efficiency

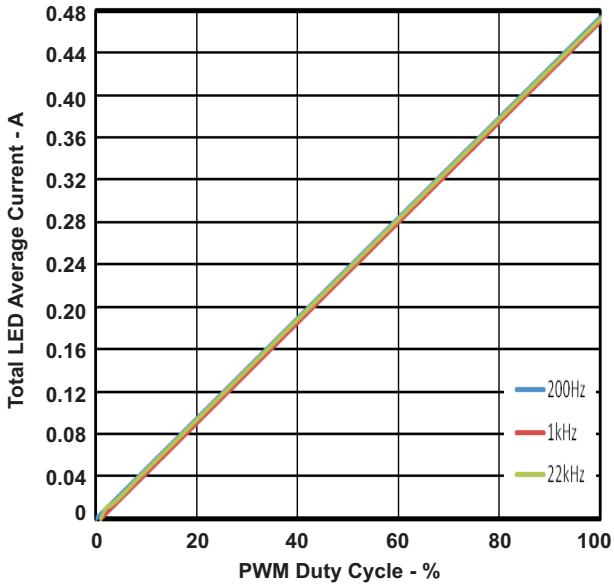


Figure 4. Dimming Linearity

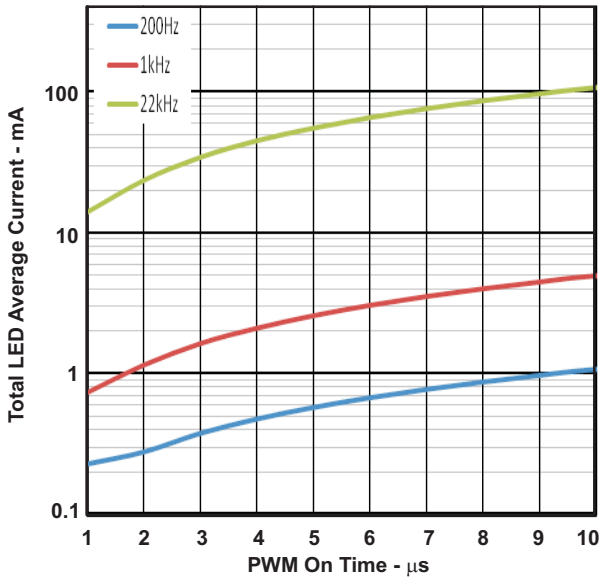


Figure 5. Dimming With Short On Time

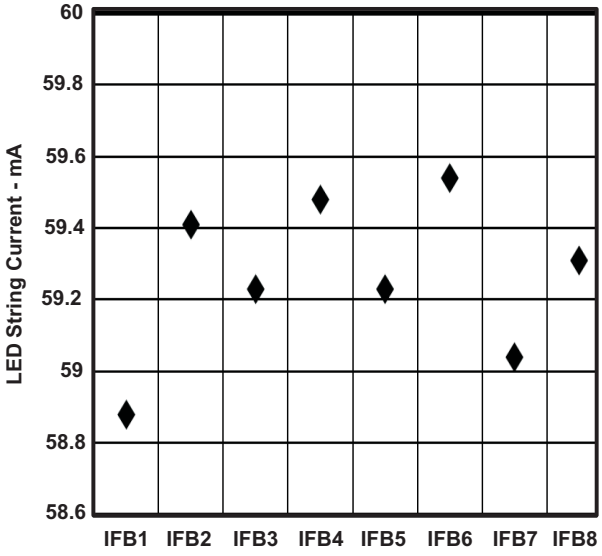


Figure 6. Current Matching

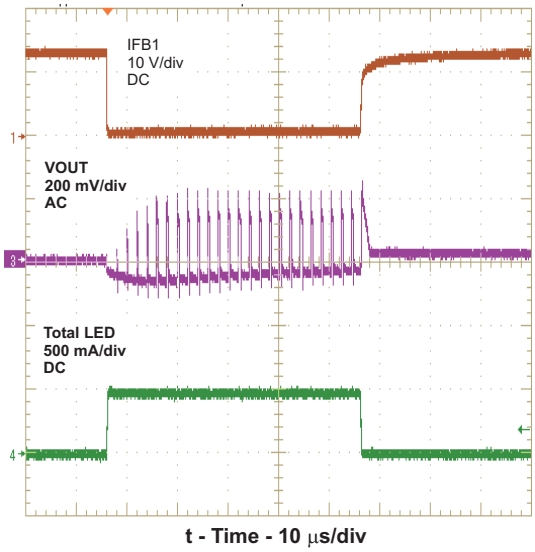


Figure 7. Dimming Waveforms

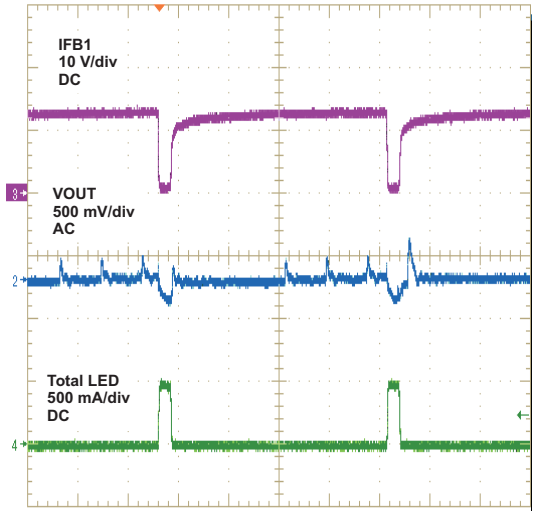


Figure 8. Dimming Waveforms

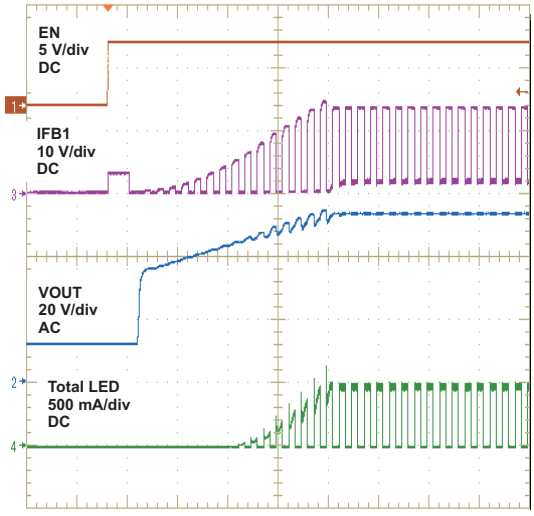


Figure 9. Startup Waveform

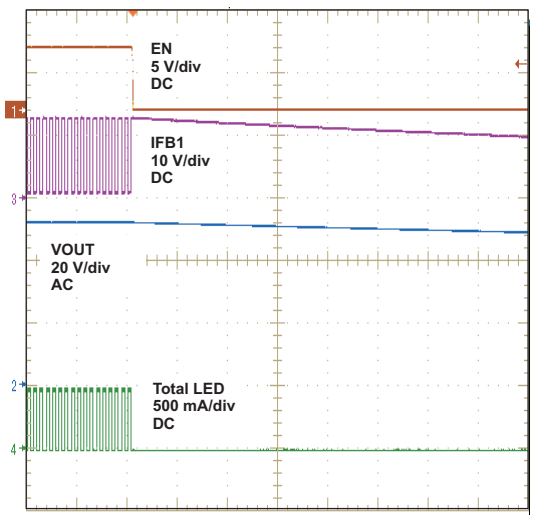


Figure 10. Shutdown Waveform

DETAILED DESCRIPTION

See the functional block diagram and Figure 1 for each section.

Supply Voltage

The TPS61199 has a built-in linear regulator to supply the IC analog and logic circuitry. The VDD pin, output of the regulator, must be connected to a 2.2µF bypass capacitor. VDD only has a current sourcing capability of 15mA. VDD voltage is ready after the EN pin is pulled high.

Boost Controller

A boost controller is shown at the top of the functional block diagram. The TPS61199 regulates the output voltage with current mode PWM (pulse width modulation) control. The control circuitry turns on an external switch FET at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as the inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the *Error Amplifier* (EA) output, the switch FET is turned off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each switching cycle. The switching frequency is programmed by the external resistor.

A ramp signal from the oscillator is added to the current ramp to provide slope compensation, shown in the *Oscillator and Slope Compensation* block. The duty cycle of the converter is then determined by the *PWM Logic* block which compares the EA output and the slope compensated current ramp. The feedback loop regulates the OVP pin to a reference voltage generated by the minimum voltage across the IFB pins. The output of the EA is connected to the COMP pin. An external RC compensation network must be connected to the COMP pin to optimize the feedback loop for stability and transient response.

The IC consistently adjusts the boost output voltage to account for any changes in LED forward voltages. In the event that the boost controller is not able to regulate the output voltage due to the minimum pulse width (t_{skip}, in the *Electrical Characterization* table), the IC enters pulse skip mode. In this mode, the device keeps the power switch off for several switching cycles to prevent the output voltage from rising above the regulated voltage. This operation typically occurs in light load condition or when the input voltage is higher than the output voltage.

Switching Frequency

The TPS61199 switching frequency can be programmed between 300kHz to 800kHz by a external resistor (R7, in Figure 1). Table 2 shows the recommended values for the resistance.

Fs (in kHz) = 80,000 / R7 (in kΩ)

Table 2. Recommended Value for Resistance

R7	F_{SW}
100 kΩ	800 kHz
160 kΩ	500 kHz

Enable And Under Voltage Lockout

The TPS61199 is enabled with the soft-start when the EN pin voltage is higher than 2.0 V; A voltage of less than 0.8 V disables the IC.

An under voltage lockout protection feature is provided. When the voltage at VIN pin is less than 7 V, the IC is switched off. The IC resumes the operation once the voltage at VIN pin recovers adjusted for hysteresis (V_{VIN_SYS}, in the *Electrical Characterization* table)

Startup

The TPS61199 has integrated soft-start circuitry to avoid any inrush current during startup. During the startup period, the output voltage rises step-by-step from the minimum voltage of LED string in 100 mV increments, shown in Figure 9. The soft-start time depends on the load and the output capacitor.

Unused LED String

If the application requires less than eight LED strings, the TPS61199 simply requires shorting the unused IFB pin to ground. The IC detects the voltage less than 0.3 V and immediately disables the string during startup. Refer to Figure 12.

Program LED Full-Scale Current

The eight current sink regulators embedded in the TPS61199 can be configured to provide up to a maximum of 70mA per string. The current must be programmed to the expected full-scale LED current by the ISET pin resistor, (R6, in Figure 1) using Equation 1.

$$I_{LED} = \frac{V_{ISET}}{R6} \times K_{ISET} \quad (1)$$

Where:

K_{ISET} = Current multiple (1990 TYP, in the *Electrical Characterization* table)

V_{ISET} = ISET pin voltage (1.229V TYP, in the *Electrical Characterization* table)

PWM Dimming

LED brightness dimming is set by applying an external PWM signal of 100Hz to 22kHz to the PWM pin. Varying the PWM duty cycle from 0% to 100% adjusts the LED from minimum to maximum brightness respectively. The minimum on time of the LED string is 1 µsec; thus the TPS61199 has a dimming ratio of 5000:1 at 200Hz. Refer to Figure 5 for dimming ratio in other dimming frequency.

When the PWM voltage is pulled low, the IC will turn off the LED strings and keep the boost converter output at the same level as when PWM is high. Thus, the TPS61199 limit the output ripple due to the load transient that occurs during PWM dimming.

Drive High Current LED

For applications requiring LEDs rated for more than 70mA, it is acceptable to tie two or more IFB pins together as shown in Figure 13.

Protection

1. Switch current limit protection using the ISNS pin

   The TPS61199 monitors the inductor current through the voltage across a sense resistor (R1 in Figure 1) in order to provide current limit protection. During the switch FET on period, when the voltage at ISNS pin rises above 160 mV (VISNS in the *Electrical Characterization* table), the IC turns off the FET immediately and does not turn it back on until the next switch cycle. The switch current limit is equal to 160mV / R1.

2. LED open protection

   When one of the LED strings is open, the boost output rises to the clamp threshold voltage (see the Output over-voltage protection using the OVP pin section). The IC detects the open string by sensing no current on the corresponding IFB pin. As a result, the IC deactivates the open IFB pin and removes it from the voltage feedback loop. Afterwards, the output voltage returns to the voltage required for the connected WLED strings. The IFB pin currents of the connected strings remain in regulation during this process.

   If all the LED strings are open, the IC repeatedly attempts to restart until the fault is cleared.

3. LED short-across protection using the FBP pin

   If one or several LEDs short in one string, the corresponding IFB pin voltage rises but continues to sink the LED current, causing increased IC power dissipation. To protect the IC, the TPS61199 provides a programmable LED short-across protection feature with threshold voltage that can be programmed by properly sizing the resistor on the FBP pin (See R5 in Figure 1) using the following equation.

$$V_{LED\_short} = \frac{R5}{R6} \times 1.229V \quad (2)$$

If any IFB pin voltage exceeds the threshold (V_{LED_short}), the IC turns off the corresponding current sink and removes this IFB pin from the output voltage regulation loop. Current regulation of the remaining IFB pins is not affected.

If the voltage on all the IFB pins exceed the threshold, the IC repeatedly attempts to restart until the fault is cleared.

4. IFB over-voltage protection

   When any of IFB pin reaches the threshold (V_{OVP_IFB}), the IC stops switching immediately to protect from damage. The IC will re-start when IFB pin voltage falls below the threshold. The time delay depends on how quickly IFB voltage can fall. It is usually determined by the amount of output capacitance and load.

5. Output over-voltage protection using the OVP pin:

   Use a resistor divider to program the clamp threshold voltage as follows:

   (a) Compute the maximum output voltage by multiplying the maximum forward voltage ($V_{FWD(MAX)}$) and number (n) of series LEDs. Add 1V to account for regulation and resistor tolerances and load transients.

   $$V_{OUTMAX} = V_{FLED\_MAX} \times \text{Number} + 1V \quad (3)$$

   (b) The recommended bottom feedback resistor (R3, in the) at 10k. Calculate the top resistor (R2, in the Figure 1) using the following equation

   $$R2 = \left(\frac{V_{OUTMAX} + 1V}{2.95V} - 1 \right) \times R3 \quad (4)$$

   When the IC detects that the OVP pin exceeds 2.95V, indicating that the output voltage has exceeded the clamp threshold voltage, the IC clamps the output voltage to the set threshold.

   When the OVP pin voltage is higher than 3.0V, indicating that the output is higher than the clamp threshold voltage due to transients or high voltage noise spike coupling from external circuits, the IC shuts down the boost controller until the output drops below the clamp threshold voltage.

6. Output short to ground protection

   When the inductor peak current reaches twice the switch current limit in each switch cycle, the IC immediately disables the boost controller until the fault is cleared. This protects the IC and external components from damage if the output is shorted to ground.

7. Thermal Protection

   When the IC junction temperature is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. The device automatically restarts when the junction temperature falls back to less than 150°C, with approximate 15°C hysteresis.

APPLICATION INFORMATION

Inductor Selection

The TPS61199 is designed to work with inductor values between 10µH to 47µH. Running the controller at higher switching frequencies allows the use of smaller and/or lower profile inductors in the 10µH range. Running the controller at slower switching frequencies requires the use of larger inductors, near 47µH, to maintain the same inductor current ripple but may improve overall inefficiency due to smaller switching losses. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. In a boost regulator, the inductor peak current can be calculated with Equation 5 and Equation 6.

$$I_{L_{Peak}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{I_{PP}}{2} \quad (5)$$

$$\Delta I_L = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_{SW}} \quad (6)$$

Where:

V_{OUT} = output voltage

I_{OUT} = total LED current

V_{IN} = input voltage

η = power conversion efficiency, use 85% for TPS61199 applications

L = inductor value

F_{SW} = switching frequency

Select an inductor with a saturation current over the calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum total LED current. Select an inductor with a saturation current at least 30% higher the calculated peak current to account for load transients when dimming. Table 2 lists the recommended inductors

Table 3. Recommended Value for Inductor

	L(µH)	DCR (mΩ)	I_{SAT} (A)	SIZE (LxWxH mm)	MFR.
CDRH127/HPNP-220M	22	48.8	5.6	12.5 x 12.5 x 8.0	Sumida
SLF12575T- 220M	22	26.3	4	12.5 x 12.5 x 7.5	TDK
#B953AS-220M	22	46	3.6	12.8 x 12.8 x 6.8	TOKO

Schottky Diode

The TPS61199 demands a high-speed rectification for optimum efficiency. Ensure theat the diode's average and peak current rating exceed the output LED current and inductor peak current. In addition, the diode's reverse breakdown voltage must exceed the application output voltage. Therefore, the VISHAY SS5P9 is recommended.

Switch MOSFET And Gate Driver Resistor

The TPS61199 demands a power N-MOSFET (See Q1 in Figure 1) as a switch. The voltage and current rating of the MOSFET must be higher than the application output voltage and the inductor peak current. The applications benefits from the addition of a resistor (See R8 in Figure 1) connected between the GDRV pin and the gate of the switching MOSFET. With this resistor, the load regulation between LED dimming on and off period and EMI are improved. A 3-Ω resistor value is recommended. The TPS61199 exhibits lower efficiency when the resistor value is above 3Ω.

Current Sense and Current Sense Filtering

R1 determines the correct over current limit protection. To choose the right value of R1, start with the total system power needed Pout. Input current Iin = Pout / (Vin * efficiency). Efficinecy can be estimated from Figure 3. The second step is to calculate the inductor ripple current based on the inductor value L.

dIL = Vin * D / (fs * L) where, D = 1 - Vin/Vo

So the peak current Ipk = Iin + dIL/2. The maximum R1 can now be calculated as,

R1 = VISNS / Ipk

It is recommended to add 20% or more margin to account for component variations.

A small filter placed on the ISNS pin improves performance of the converter (See R9 and C6 in Figure 1). The time constant of this filter should be approximately 100ns. The range of R9 should be from about 100Ω to 1kΩ for best results. The C6 should be located as close as possible to the ISNS pin to provide noise immunity.

Output Capacitor

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability of the whole system. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$V_{ripple_C} = \frac{D_{MAX} \times I_{OUT}}{F_{SW} \times C_{OUT}} \quad (7)$$

Where $V_{ripplec}$ is the peak to peak output ripple, and D_{MAX} is the duty cycle of the boost converter. D_{MAX} is equal to approximately (V_{OUT_MAX} - V_{IN_MIN}) / V_{OUT_MAX} in applications.

Care must be taken when evaluating a capacitor's derating under dc bias. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance in the recommendation table.

The ESR impact on the output ripple must be considered as well if tantalum or electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the Vripple is:

$$V_{ripple_{ESR}} = I_{L_{Peak}} \times ESR \quad (8)$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. Therefore, three electrolytic capacitors (UPW2A330MPD6, Nichicon) in parallel reduces the total ESR, shown as Figure 1.

In typical application, The output requires a capacitor in the range of 10µF to 100µF. The output capacitor affects the small signal control loop stability of the boost converter. If the output capacitor is below the range, the boost regulator may potentially become unstable.

Loop Consideration

The COMP pin on the TPS61199 is used for external compensation, allowing the loop response to be optimized for each application. The COMP pin is the output of the internal transconductance amplifier. The external resistor R4, along with ceramic capacitors C4 and C5, are connected to the COMP pin to provide poles and zero. The poles and zero, along with the inherent pole and zero in a peak current mode control boost converter, determine the closed loop frequency response. This is important to converter stability and transient response. For most of the applications, the recommended value of 10kΩ for R4, 100nF for C4 and 470pF for C5 are sufficient. For applications with different components or requirements, please refer to application note SLVA452 "Compensating the Current Mode Boost Converter" for guidance on selecting different compensation components.

Layout Consideration

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The VDD capacitor, C3 (see in Figure 1) is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits. It should be placed as close as possible between the VDD and GND pins to prevent any noise insertion to digital circuits. The switch node at the drain of Q1 carries high current with fast rising and falling edges. Therefore, the connection between this node to the inductor and the schottky diode should be kept as short and

wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the GND pin since there is large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separate from power ground traces and connect them together at a single point, for example on the thermal pad in the PWP package. Resistors R5, R6, and R7 in the Typical Application Circuits are LED short protection threshold current setting and switching frequency programming resistors. To avoid unexpected noise coupling into the pins and affecting the accuracy, these resistors need to be close to the pins with short and wide traces to GND. In PWP package, The thermal pad needs to be soldered on to the PCB and connected to the GND pin of the IC. Additional thermal via can significantly improve power dissipation of the IC.

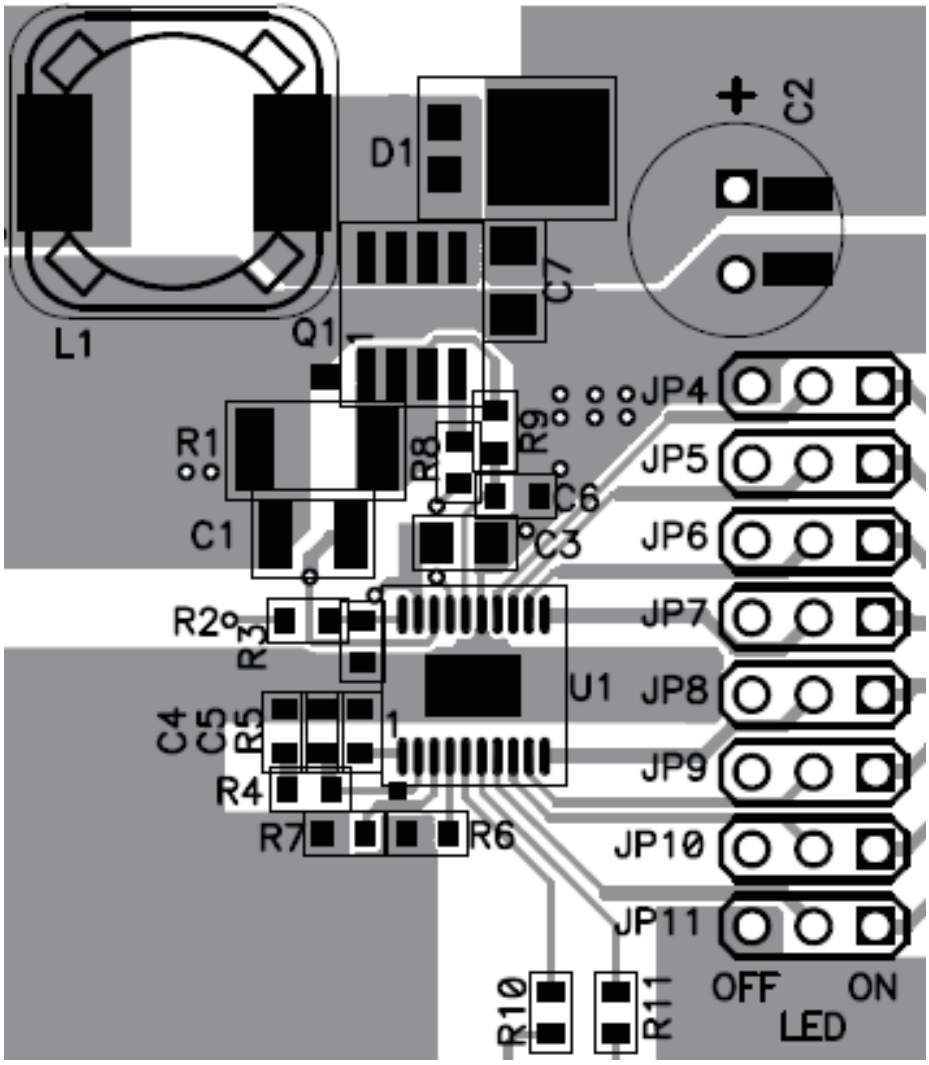


Figure 11. Recommended PCB Layout

ADDITIONAL APPLICATION CIRCUITS

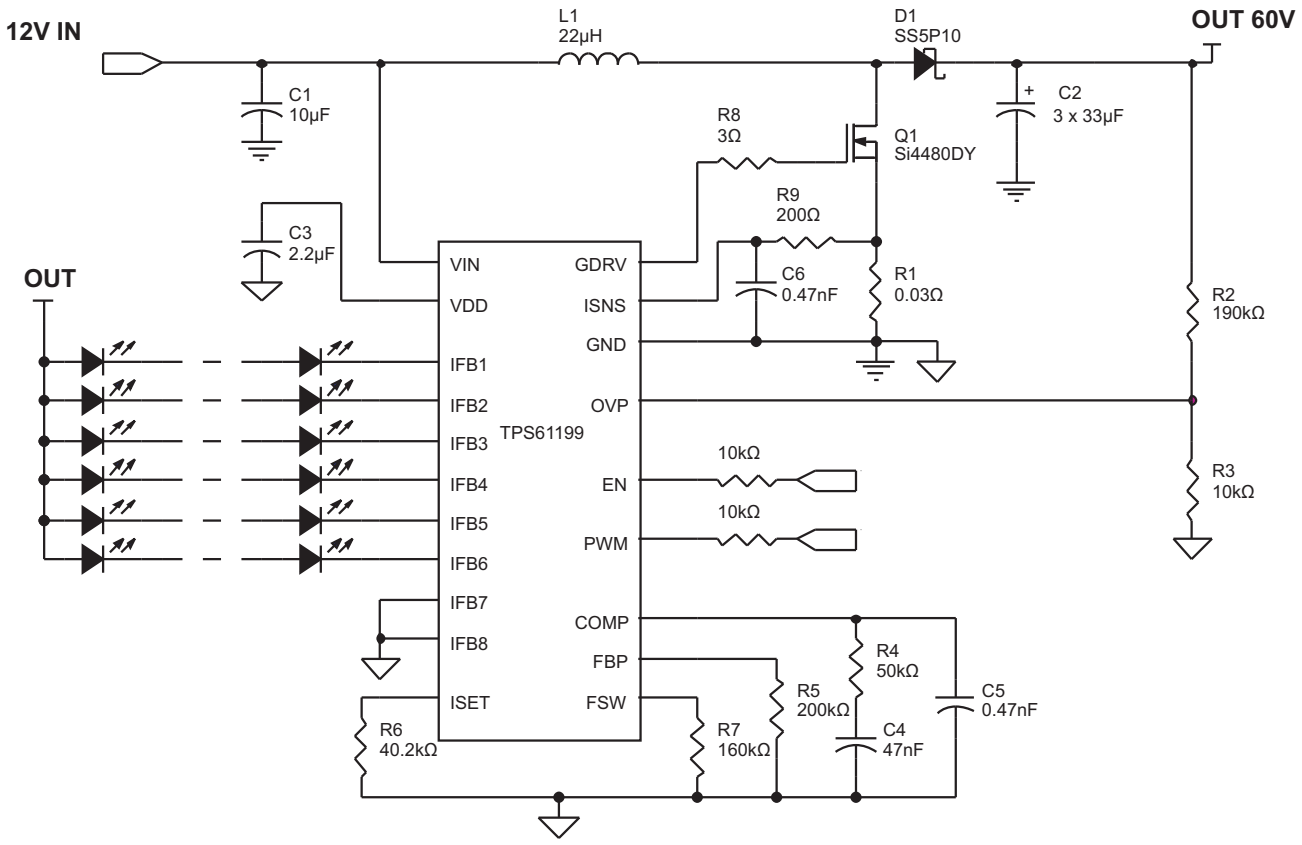


Figure 12. Six LED Strings Application

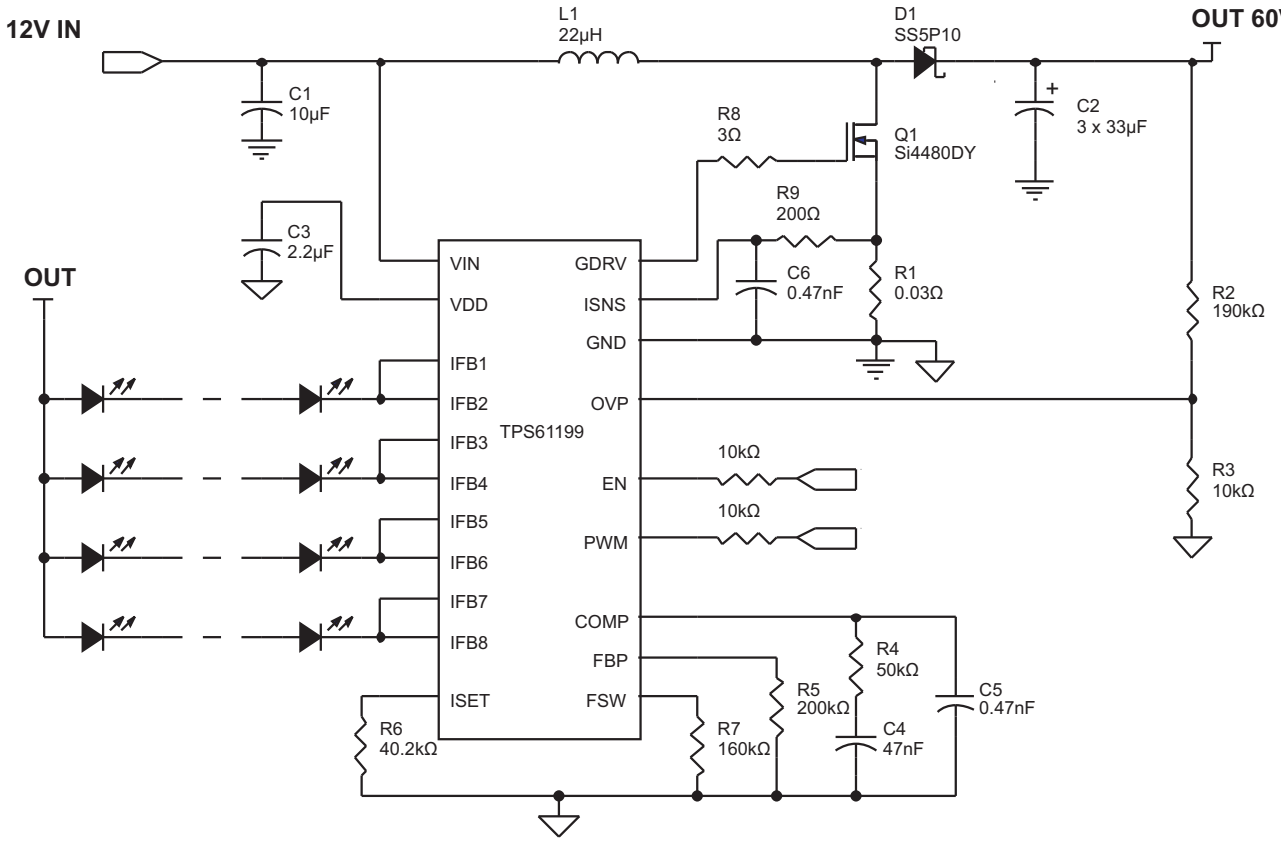


Figure 13. Four LED Strings with 130mA Current Application

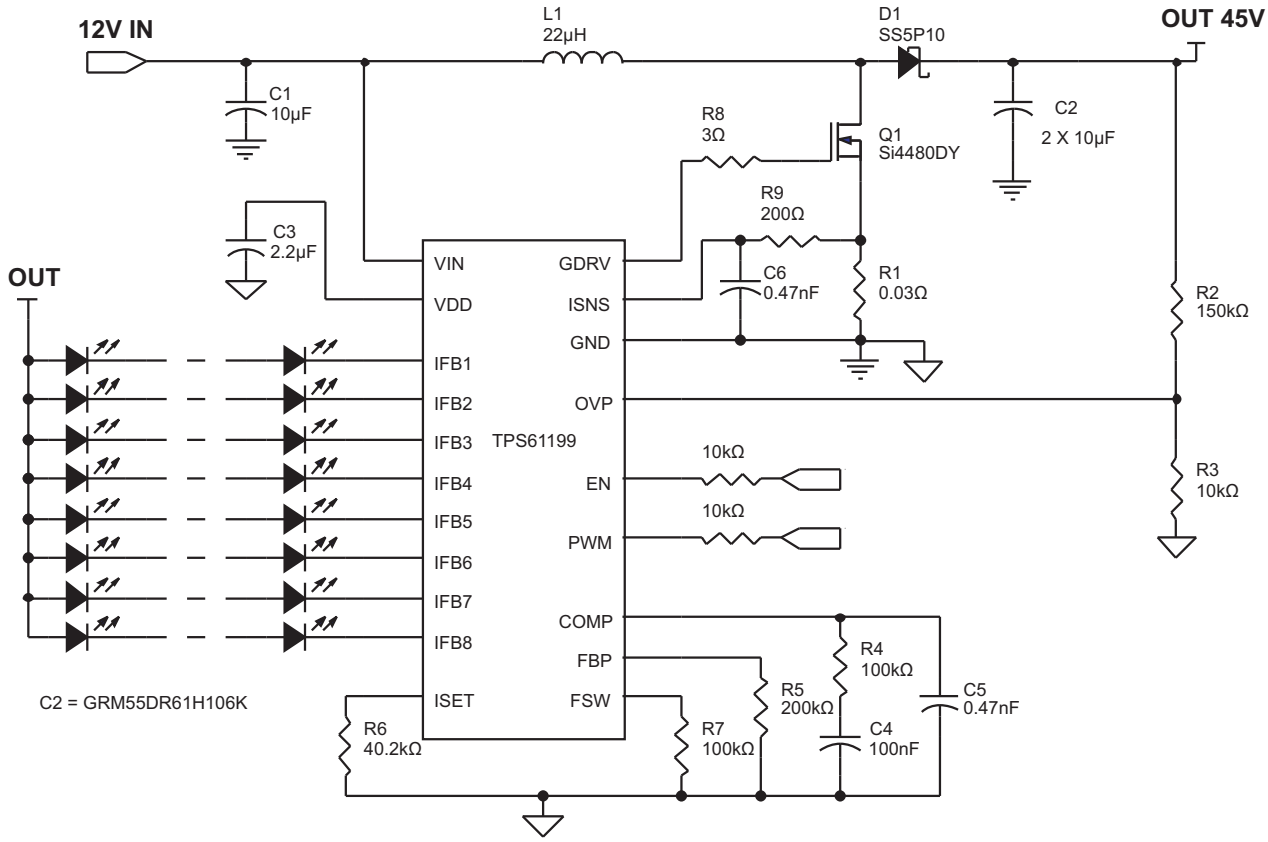


Figure 14. 112-LED Driver Application with Ceramic Output Capacitor

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS61199NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS61199PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS61199PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

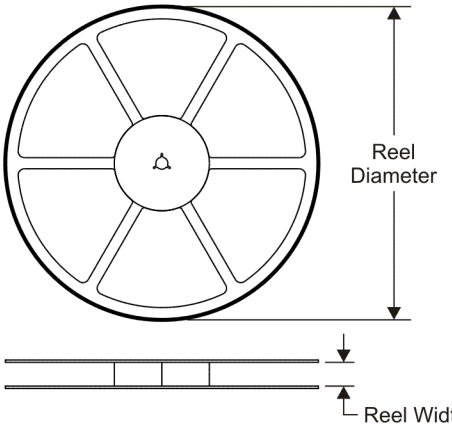
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

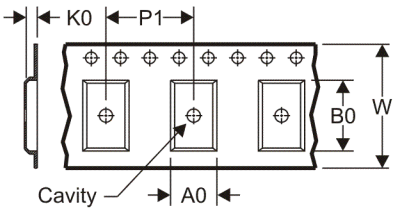
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

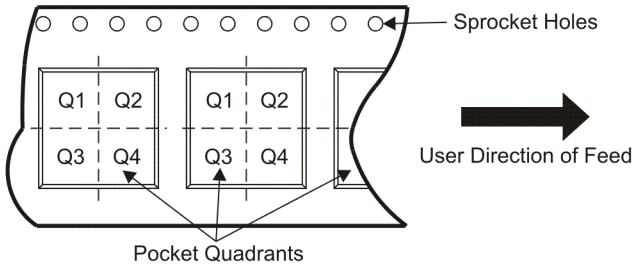


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

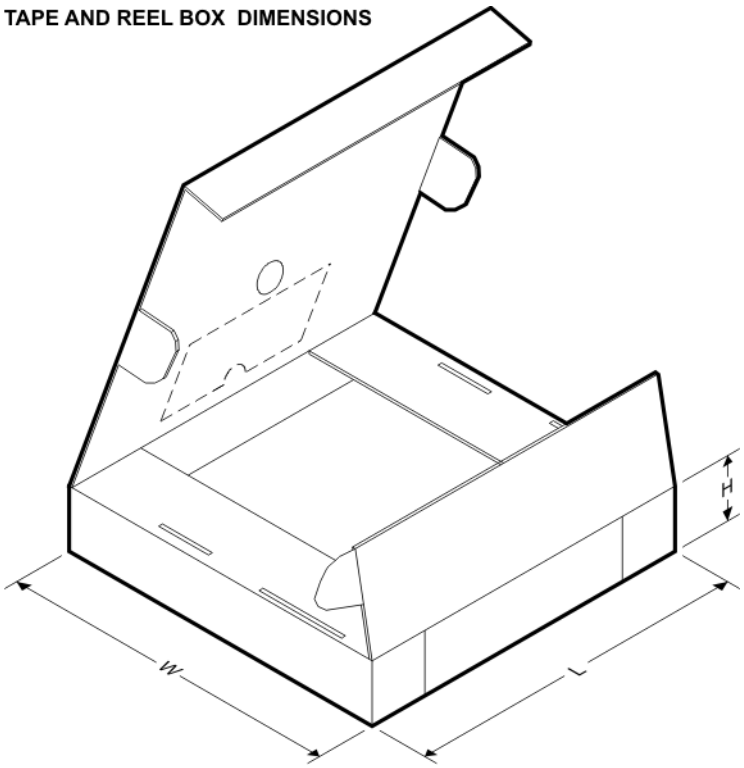
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61199NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

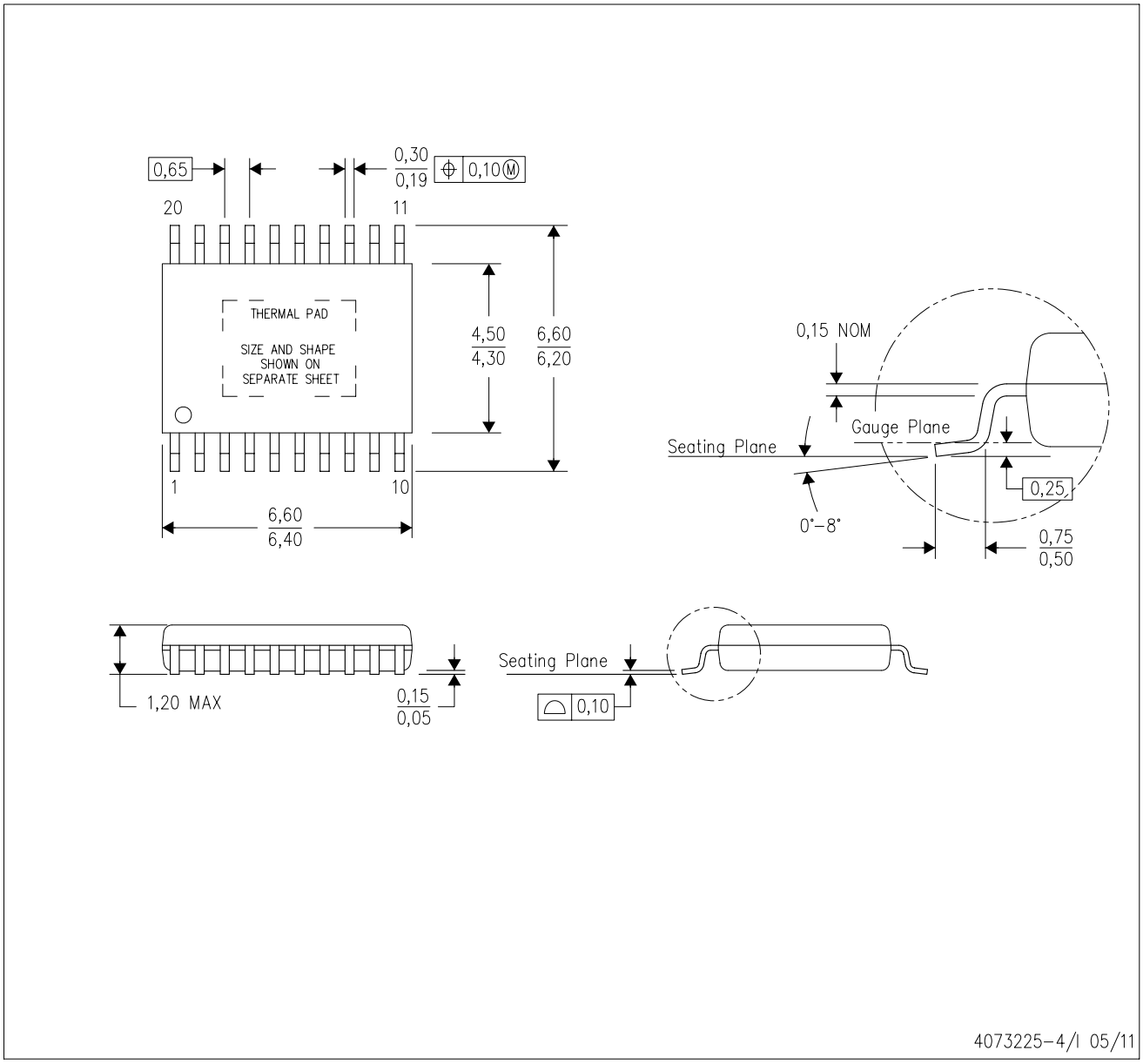
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61199NSR	SO	NS	20	2000	346.0	346.0	41.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

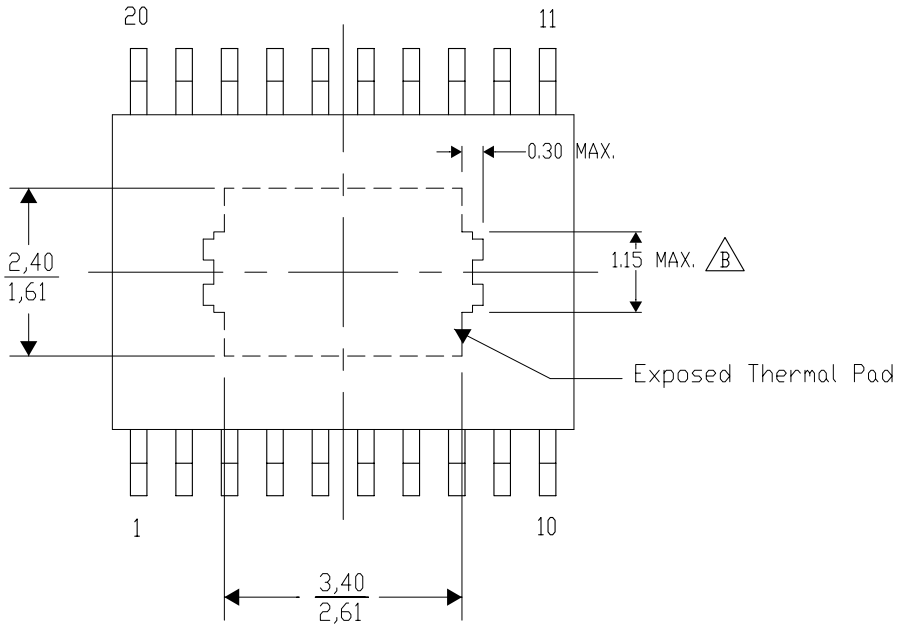
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

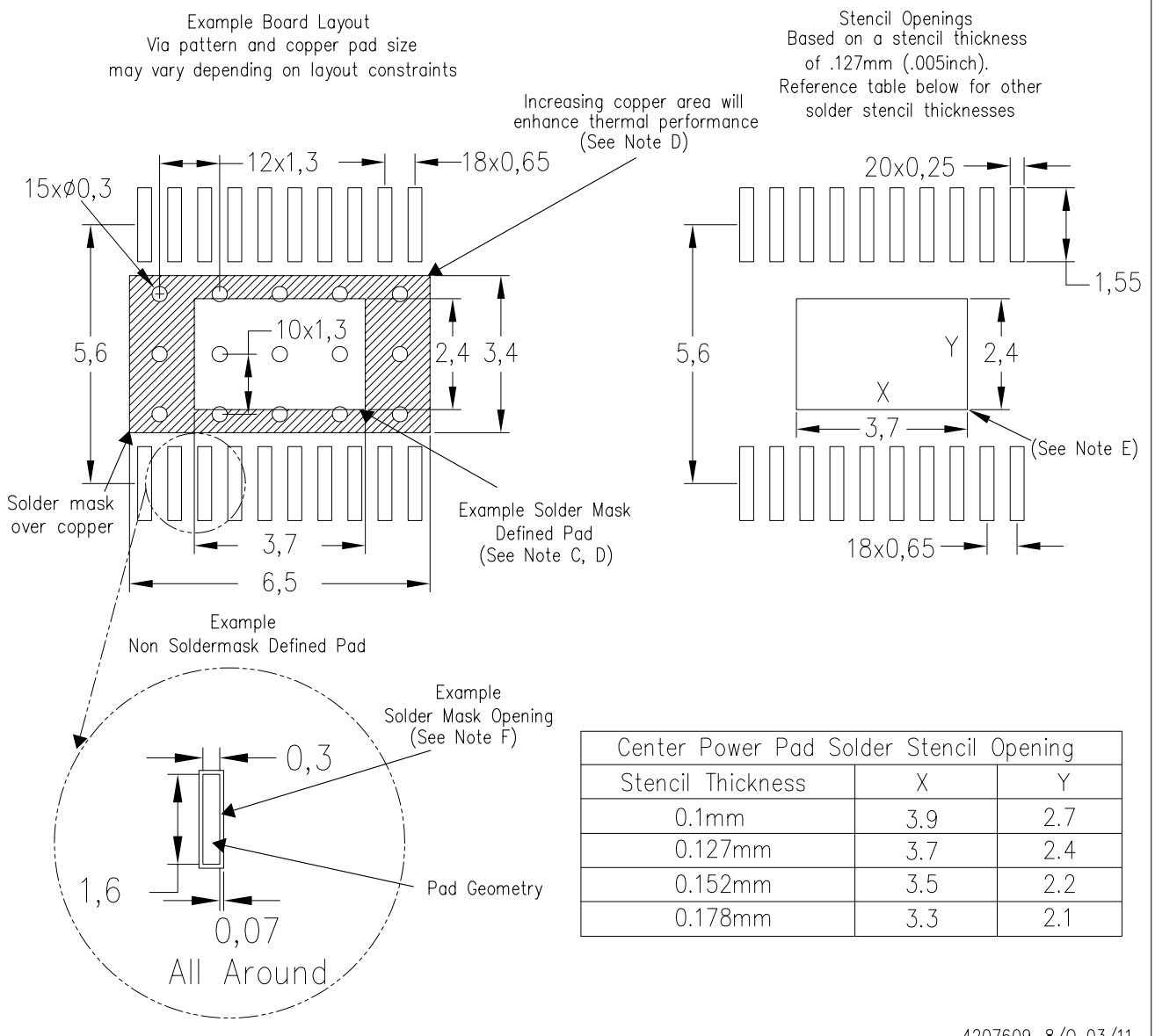
4206332–8/W 05/11

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/Q 03/11

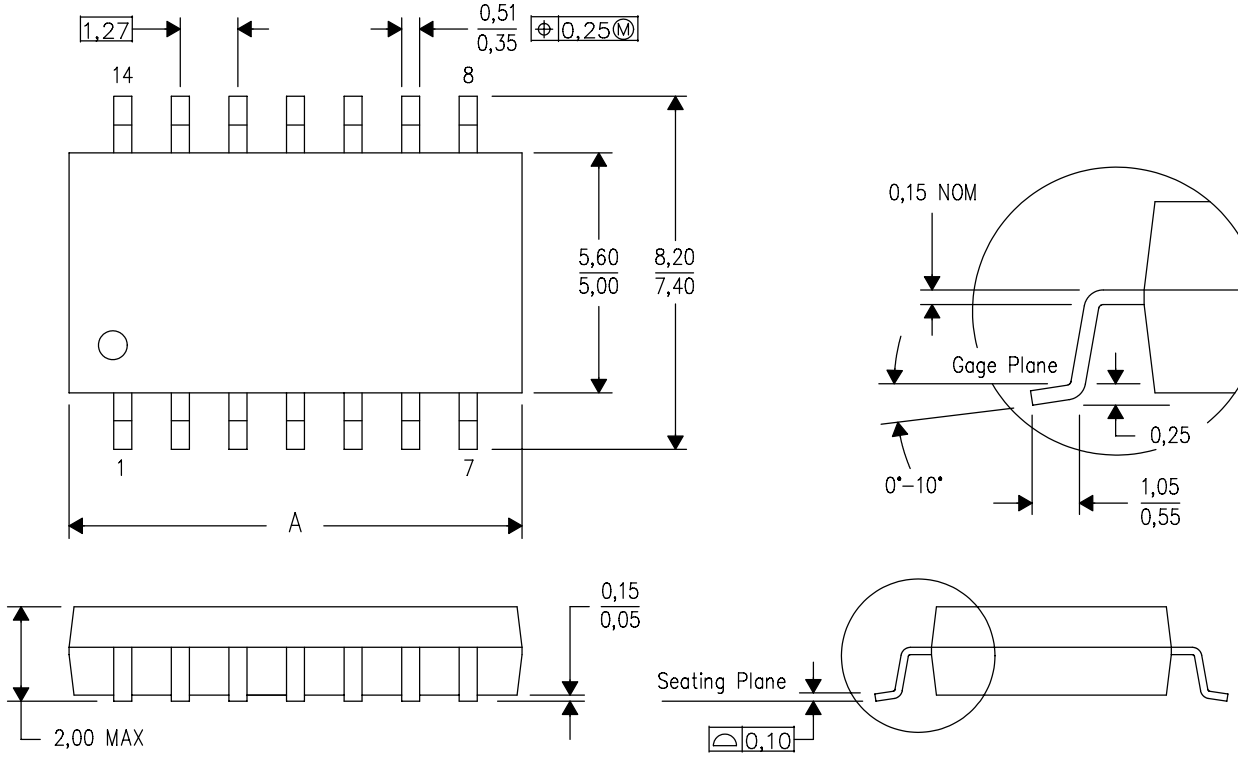
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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